WHAT IS CLAIMED IS:

1. A method of forming a Type-I transistor and a Type-II transistor suitable for a liquid crystal display (LCD), comprising:

providing a substrate;

forming a first polysilicon layer and a second polysilicon layer corresponding to the Type-I transistor and the Type-II transistor respectively on the substrate;

blanketly forming a gate insulating layer on the first polysilicon layer, the second polysilicon layer, and the substrate;

forming a first gate and a second gate on the gate insulating layer respectively corresponding to the first polysilicon layer and the second polysilicon layer;

performing a first doping using a first type dopant to form a first heavily doped region in the first polysilicon layer beside the first gate; and

performing a second doping using a second type dopant to simultaneously form a second heavily doped region in the second polysilicon layer beside the second gate and form a lightly doped region in parts of the

first heavily doped region beside the first gate, wherein the dosage of the second type dopant is smaller than that of the first type dopant.

2. The method according to claim 1, wherein the method further comprises the step of forming a buffer layer on the substrate prior to the step of forming a first polysilicon layer and a second polysilicon layer.

3. The method according to claim 1, wherein following the step of performing a light doping of the Type-I transistor and a second heavy doping of the Type-II transistor, the method further comprises:

forming an inner dielectric layer on the gate oxide, the first gate and the second gate;

selectively exposing the first heavily doped region, the second heavily doped region, the first gate and the second gate; and

forming an electrode to be electrically connected to the first heavily doped region, the second heavily doped region, the first gate and the second gate which have already been exposed;

wherein the thickness of the inner dielectric layer is about 500 ~ 7000 angstroms, and the electrode comprises Mo, Cr or Ti/Al/Ti.

4. The method according to claim 3, wherein following the step of forming the electrode, the method further comprises:

forming a patterned passivation layer on the inner dielectric layer and the electrode, wherein the patterned passivation layer exposes part of the electrode of the Type-I transistor situated in a pixel region of the LCD; and

forming a transparent electrode to be electrically connected to the exposed part of the electrode of the Type-I transistor;

wherein the transparent electrode comprises indium-tin oxide (ITO).

5. The method according to claim 1, wherein the thickness of the first polysilicon layer and the second polysilicon layer is about 200 ~ 1000 angstroms, the thickness of the gate oxide layer is about 500 ~ 1500 angstroms, and the first gate and the second gate comprise Mo, Cr or Ti/Al/Ti.

6. The method according to claim 1, wherein the Type-I transistor is an NMOS transistor while the Type-II transistor is a PMOS transistor, the first type dopant is a phosphorus dopant, and the second type dopant is a boron dopant.

7. The method according to claim 1, wherein the Type-I transistor is a

PMOS transistor while the Type-II transistor is an NMOS transistor, the first type dopant is a boron dopant, and the second type dopant is a phosphorus dopant.

8. The method according to claim 1, wherein the first heavily doped region is source and drain of the Type-I transistor, and the second heavily doped region is source and drain of the Type-II transistor.

9. The method according to claim 1, wherein the dosage of first type dopant is about 3el3 dosage/cm^2 ~ 5el5 dosage/cm^2.

10. The method according to claim 1, wherein the dosage of second type dopant is about 3el3 dosage/cm^2 ~ 5el5 dosage/cm^2.

11. A method of forming a Type-I transistor and a Type-II transistor suitable for a LCD, comprising:

providing a substrate;

forming a first polysilicon layer and a second polysilicon layer corresponding to the Type-I transistor and the Type-II transistor respectively on the substrate;

blanketly forming a gate insulating layer on the first polysilicon layer,

the second polysilicon layer, and the substrate;

forming a first gate and a second gate on the gate insulating layer respectively corresponding to the first polysilicon layer and the second polysilicon layer;

forming a first patterned photoresist layer covering up entire region of the Type-II transistor;

performing a first doping using a first type dopant to form a first heavily doped region in the first polysilicon layer beside the first gate using the first photoresist layer as a mask; and

forming a second patterned photoresist layer covering up the source/drain region of the Type-I transistor;

performing a second doping using a second type dopant to simultaneously form a second heavily doped region in the second polysilicon layer beside the second gate and form a lightly doped region in parts of the first heavily doped region beside the first gate by using the second photoresist layer as a mask, wherein the dosage of the second type dopant is smaller than that of the first type dopant.

12. The method according to claim 11, wherein the method further comprises the step of forming a buffer layer on the substrate prior to the step of forming a first polysilicon layer and a second polysilicon layer.

13. The method according to claim 11, wherein following the step of performing a light doping of the Type-I transistor and a second heavy doping of the Type-II transistor, the method further comprises:

forming an inner dielectric layer on the gate oxide, the first gate and the second gate;

selectively exposing the first heavily doped region, the second heavily doped region, the first gate and the second gate; and

forming an electrode to be electrically connected to the first heavily doped region, the second heavily doped region, the first gate and the second gate which have already been exposed;

wherein the thickness of the inner dielectric layer is about 500 ~ 7000 angstroms, and the electrode comprises Mo, Cr or Ti/Al/Ti.

14. The method according to claim 13, wherein following the step of forming the electrode, the method further comprises:

forming a patterned passivation layer on the inner dielectric layer and the electrode, wherein the patterned passivation layer exposes part of the electrode of the Type-I transistor situated in a pixel region of the LCD; and

forming a transparent electrode to be electrically connected to the exposed part of the electrode of the Type-I transistor;

wherein the transparent electrode comprises indium-tin oxide (ITO).

15. The method according to claim 11, wherein the thickness of the first polysilicon layer and the second polysilicon layer is about 200 ~ 1000 angstroms, the thickness of the gate oxide layer is about 500 ~ 1500 angstroms, and the first gate and the second gate comprise Mo, Cr or Ti/Al/Ti.

16. The method according to claim 11, wherein the Type-I transistor is an NMOS transistor while the Type-II transistor is a PMOS transistor, the first type dopant is a phosphorus dopant, and the second type dopant is a boron dopant.

17. The method according to claim 11, wherein the Type-I transistor is a PMOS transistor while the Type-II transistor is an NMOS transistor, the first type dopant is a boron dopant, and the second type dopant is a phosphorus dopant.

18. The method according to claim 11, wherein the first heavily doped region is source and drain of the Type-I transistor, and the second heavily doped region is source and drain of the Type-II transistor.

19. The method according to claim 11, wherein the dosage of first type dopant is about 3el3 dosage/cm^2 ~ 5el5 dosage/cm^2.

20. The method according to claim 11, wherein the dosage of second type dopant is about 3el3 dosage/cm^2 ~ 5el5 dosage/cm^2.

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